NEW UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Docket No. M4065.0226/P226
Total pages in this submission

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

DIE ATTACH CURING METHOD FOR BGA PRODUCT

and invented by:

Tongbi Jiang

IF A CONTINUATION APPLICATION, check appropriate box and supply requisite information:

☐ Continuation ☐ Divisional

☐ Continuation-in-part (CIP) of prior application No.: _____

Enclosed are:

Application Elements

1. [X] Filing fee as calculated and transmitted as described below
2. [X] Specification having 15 pages(s) and including the following:
   - a. [X] Descriptive title of the invention
   - b. [ ] Cross references to related applications *(if applicable)*
   - c. [ ] Statement regarding Federally-sponsored research/development *(if applicable)*
   - d. [ ] Reference to microfiche appendix *(if applicable)*
   - e. [X] Background of the invention
   - f. [X] Brief summary of the invention
   - g. [X] Brief description of the drawings *(if drawings filed)*
   - h. [X] Detailed description
   - i. [X] Claims as classified below
   - j. [X] Abstract of the disclosure

Application Elements (continued)

3. [X] Drawing(s) *(when necessary as prescribed by 35 U.S.C. 113)*

   [ ] Formal [X] Informal Number of sheets: 5

4. [X] Oath or Declaration

   a. [X] Newly executed (original or copy) [ ] Unexecuted

   b. [ ] Copy from a prior application (37 C.F.R. 1.63(d) *(for continuation/divisional applications only)*

   c. [ ] With Power of Attorney [X] Without Power of Attorney

5. [ ] Incorporation by reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Computer program in microfiche

7. [ ] Genetic sequence submission *(if applicable, all must be included)*

   a. [ ] Paper copy

   b. [ ] Computer readable copy

   c. [ ] Statement verifying identical paper and computer readable copies

Accompanying Application

8. [X] Assignment papers *(cover sheet & document(s))*

9. [X] 37 C.F.R. 3.73(b) statement *(when there is an assignee)*

10. [ ] English translation document *(if applicable)*

11. [ ] Information Disclosure Statement/PTO-1449 [ ] Copies of IDS citations

12. [ ] Preliminary Amendment

13. [X] Acknowledgment postcard

14. [ ] Certified copy of priority document(s) *(if foreign priority is claimed)*

15. [ ] Certificate of Mailing

    [ ] First Class [ ] Express Mail (Label No.: _____)

16. [ ] Small Entity statement(s) -- # submitted _____ *(if Small Entity status claimed)*

Accompanying Application (continued)

17. ☐ Additional enclosures *(please identify below):*

Fee Calculation and Transmittal

The filing fee for this utility patent application is calculated and transmitted as follows:

☒ Large Entity ☐ Small Entity

CLAIMS AS FILED					
For	**# Filed**	**# Allowed**	**# Extra**	**Rate**	**Fee**
Total Claims	30	- 20 =	10	x $18.00	$180.00
Independent Claims	3	- 3 =	0	x $78.00	
Multiple Dependent Claims (check if applicable)			☐		
Other Fees (specify purpose): Recordation Form Cover Sheet					$40.00
				BASIC FEE	$690.00
				TOTAL FILING FEE	$910.00

☒ A check in the amount of $910.00 to cover the total filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and Deposit Account No. 4 - 1073 as described below. A duplicate copy of this sheet is enclosed.

☐ Charge the amount of _____ as filing fee.

☒ Credit any overpayment.

☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.

☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.31(b).

Dated: January 18, 2000

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Docket No.: M4065.0226/P226
Micron No.: 98-956

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR U.S. LETTERS PATENT

Title:

DIE ATTACH CURING METHOD FOR SEMICONDUCTOR DEVICE

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DIE ATTACH CURING METHOD FOR SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

The present invention generally relates to semiconductor device fabrication. More particularly, the present invention relates to the curing of an adhesive material used in affixing solder masks to semiconductor chips.

BACKGROUND OF THE INVENTION

Some conventional semiconductor devices include chips having a solder mask and printed or screened-on conductive traces for wirebonding to a ball grid array (BGA). Generally, the solder mask is affixed to the chip by an adhesive material. Typically, the adhesive material is applied to the chip and allowed to cure prior to deposition of the solder mask. Currently utilized adhesive materials cure at a temperature in excess of 150°C.

Most solder masks are formed from a liquid photoimageable material. Two popular solvents used in forming liquid photoimageable solder masks are diethylene glycol monoethyl ether acetate (DGMEA) and dipropylene glycol monoethyl ether (DGME). Often a heavy aromatic naphtha also is used as a photoinitiator. All of these materials boil at relatively high temperatures. Specifically, DGMEA boils at 219°C, DGME boils at 90°C, and naphtha boils at between 80° and 220°C.

Some currently used fabrication methods cure the adhesive material along with the solder mask. During such methods, a cure of about one hour at 150°C of the liquid photoimageable solder mask is carried out. Such a cure serves to drive the low temperature volatile components of the solder mask, i.e., from the DGMEA and/or

DGME, out, leaving behind the higher temperature volatiles to outgas later when the temperature of the device in operation reaches a sufficient outgassing temperature. Since the cure time and temperature are insufficient to cure the adhesive material, later outgassing may induce voids in the adhesive material. Voids are capable of entrapping moisture, causing the semiconductor package to fail an environmental test. Further, outgassing contaminates the bond pads, resulting in a low bond yield. In addition, curing at high temperatures creates thermal stresses between the adhesive material and the die which are particularly problematic for large and/or thin semiconductor device packages.

There exists a need for a curing methodology which inhibits the effects of outgassing on adhesive material, thereby reducing voiding and the collection of moisture within the adhesive material, as well as which reduces thermal stress on the device package and contamination of the bond pads.

SUMMARY OF THE INVENTION

The present invention provides a semiconductor device having a solder mask, a die and an adhesive layer affixing the die to the solder mask. The adhesive layer is cured at a temperature below about 100°C.

The present invention also provides a semiconductor device having a solder mask, a die, electrical contacts on the solder mask and the die, each contact on the die being wire bonded to a respective contact on the mask, and an adhesive layer affixing the die to the solder mask. The adhesive layer is cured at a temperature between about

20°C and about 50° higher than a glassy temperature of the adhesive layer and the curing temperature is below about 100°C.

The present invention further provides a semiconductor package including a chip, a solder mask affixed to a die by an adhesive layer which is cured at a temperature below about 100°C, the die being electrically connected to the chip, and a mold encapsulating the chip, solder mask and die.

The present invention further provides a method of forming a semiconductor device. The method includes the steps of affixing a solder mask to a semiconductor die with an adhesive layer, and curing the adhesive layer by exposing the adhesive layer to a temperature no greater than 100°C.

These and other advantages and features of the invention will be more readily understood from the following detailed description of the invention which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a conventionally fabricated semiconductor chip on a printed circuit board.

FIG. 2 is a cross-sectional view of a semiconductor chip on a printed circuit board fabricated in accordance with an embodiment of the invention.

FIG. 3 is a graph of the change in the modulus of elasticity of an adhesive material over a temperature range.

FIG. 4 is a graph of the change in the coefficient of thermal expansion of an adhesive material over a temperature range.

FIG. 5 is a graph depicting the wire bond pull force of an 80°C cured adhesive material versus a 125°C cured adhesive material.

FIG. 6 is a graph depicting radii of curvature for various adhesive materials at various temperatures and curing times.

FIG. 7 illustrates a method of forming a semiconductor package in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 illustrates a conventionally fabricated semiconductor device 10, which includes a die 12 affixed to a solder mask 18 by an adhesive layer 14. The die 12 has contacts 20 in connection with contacts 22 on the solder mask 18. Specifically, each contact 20 is connected with a respective contact 22 through a wire bond 28. The solder mask 18 is affixed to a printed circuit board 40 or other substrate. The solder mask 18 contains DGMEA or DGME, or other materials. Further, a heavy aromatic naphtha may be used as a photoinitiator.

During the high temperature die attach adhesive curing, high temperature volatiles outgas from the solder mask 18 and/or the printed circuit board 40, forming voids 16 in the adhesive layer 14. As noted above, voids can trap moisture, causing the device 10 to fail an environmental test. Further, the outgassing may contaminate the contacts 20, 22, thereby decreasing the likelihood of a good bond therebetween.

The present invention obviates the problems caused by high temperature curing of the solder mask 18 by initially low temperature curing the adhesive layer. FIG. 2 shows a semiconductor device 100 formed in accordance with the present invention. The die 12 is affixed to the solder mask 18 by an adhesive layer 114. The layer 114 is subjected to a low temperature cure, for example, below 100°C, for a period of time to sufficiently solidify the adhesive layer 114, rendering it more impervious to the effects of outgassing.

Referring now to FIGS. 3-4, there is a correlation between both the Young's Modulus (E) and the coefficient of thermal expansion (CTE). Specifically, there is a limited temperature range at which a material changes from a flexible/pliable state to a solid. At that same limited temperature range, a material's CTE is changed. This limited temperature range is called the glassy temperature T_g. The adhesive layer 14 (FIG. 1) is formulated such that its cure temperature is greater than or equal to its glassy temperature T_g, and since it cures at about 150°C, its T_g is equal to or less than about 150°C.

The adhesive layer 114 is formulated to cure at a temperature below 100°C. A preferred formulation of the adhesive layer 114 includes one or more components which cure at or below 100°C. One such component is a resin bismaleimide. The bismaleimide may be the sole component in the layer 114 or it may be present in the adhesive layer 114 as a component. The adhesive layer 114 may include initiators which act as a catalyst to begin the curing at a lower temperature. One such initiator is peroxide, which upon being heated to a temperature below 100°C, releases free radicals. The free radicals start the chain polymerization.

Bismaleimide has a glassy temperature T_g of between about 5°C and about 10°C. To completely cure a resin, i.e., to fully cross-link the resin, a temperature of about 50°C above the glassy temperature T_g is required. Thus, an adhesive layer 114 formed of bismaleimide will cure at a temperature of about 70°C. A higher temperature would accelerate the curing process. Curing at temperatures below 100°C reduces the stresses between the adhesive layer 114 and the die 12 and strengthens the adhesive layer 114 against voids 16 caused by outgassing. Further, a low temperature cure reduces the release of volatiles which can contaminate the contacts 20, 22, and thus a low temperature cure will provide a cleaner wire bonding site at the contacts 20, 22.

One test to determine the viability of low temperature curing is to measure the wire pull force. Measuring the pull force allows one to ascertain which adhesives that are cured at low temperature perform similarly to adhesives which are cured at high temperatures. Typically, one would expect a lower force with a non-fully cured adhesive. Referring to FIG. 5, a pair of cured adhesives, B170 and D170, were stress tested. D170 is a die adhesive cured for four hours at 80°C, and B170 is a die adhesive cured at 125° for one hour (manufacturer's suggested cure profile). The force required to pull a wire bond of D170 free at 170°C is approximately 6.75 grams, which measures favorably to the 5.75 grams for the B170 adhesive. This result indicates that a low temperature cure (below 100°C) does not affect the mechanical strength of the material.

The stress of the adhesive may be determined by measuring the radius of curvature (ROC) measurement. The higher the stress of the adhesive, the lower the

ROC. FIG. 6 illustrates the radius of curvature (ROC) of an adhesive material over a variety of conditions. Table 1 illustrates the various conditions.

TABLE 1

Reference	Condition
A	cured at 125° for one hour.
A125	cured at 125° for one hour and wire bonded at 125°C.
A170	cured at 125° for one hour and wire bonded at 170°C.
C	cured at 80° for four hours.
C125	cured at 80°C for four hours and wire bonded at 125°C.
C170	cured at 80° for four hours and wire bonded at 170°C.
G1	cured at 150°C for twenty minutes.
G2	cured at 150°C for forty minutes.
G3	cured at 150°C for one hour.
G4	cured at 150°C for two hours.

As indicated in FIG. 6, the low temperature cured adhesive material 114, denoted as C, C125 and C170, shows a higher radius of curvature than the adhesive materials which were high temperature cured. As noted above, the higher the ROC the lower the stress of the adhesive

FIG. 6 also indicates that as long as the adhesion is adequate, the curing of the adhesive layer 114 does not need to be complete. More curing can be accomplished at the following processes: wire bonding, encapsulation, solder reflow, and testing. It has been determined that the adhesive layer 114 subjected to a fifty percent cure exhibits sufficient adhesive strength to pass the package assembly process.

Referring to FIG. 7, next will be described a method for fabricating a semiconductor device package. The initial step 200 is to affix the die 12 to the solder mask 18 with the adhesive material 114. Then, the adhesive material 114 undergoes a low temperature cure at step 205. As indicated above, the low temperature cure is at a temperature below 100°C. The contacts 20 are electrically connected by the wire bonds 28 to the contacts 22 at step 210. The entire assemblage is encapsulated in a mold at step 215. The molding process is typically at a high temperature, for example, greater than or equal to about 180°C. An optional post mold cure is then provided at step 220. The post mold cure is typically at about 175° for about four hours.

If the adhesive material 114 is not completely cured during the low temperature cure step 205, it will become so during the subsequent heating steps 210, 220. High temperature curing, as noted above, may introduce high thermal stress. Nonetheless, the amount of thermal stress imparted to the adhesive material 114 is reduced since at least fifty percent of the adhesive material 114 is cured at a low temperature.

The present invention provides an adhesive material which is low temperature cured, thus reducing thermal stresses and the formation of voids. The present invention further provides a method for making a semiconductor device including such an adhesive material.

While the invention has been described in detail in connection with the preferred embodiments known at the time, it should be readily understood that the invention is not limited to such disclosed embodiments. Rather, the invention can be modified to incorporate any number of variations, alterations, substitutions or

equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. Accordingly, the invention is not to be seen as limited by the foregoing description, but is only limited by the scope of the appended claims.

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A semiconductor device comprising:

a solder mask;

a die; and

an adhesive layer between said die and said solder mask, wherein said adhesive layer is at least partially cured at a temperature below about 100°C.

2. The semiconductor device of claim 1, wherein said adhesive layer is at least fifty percent cured at a temperature below about 100°C.

3. The semiconductor device of claim 1, wherein said adhesive layer is fully cured at a temperature below about 100°.

4. The semiconductor device of claim 1, wherein said adhesive layer is cured at a temperature between about 20°C and about 50° C higher than the glassy temperature of said adhesive layer.

5. The semiconductor device of claim 4, wherein said adhesive layer is cured at a temperature below about 85°C.

6. The semiconductor device claim 5, wherein said adhesive layer comprises a material with a glassy temperature between about 5°C and about 20°C.

7. The semiconductor device of claim 6, wherein said adhesive layer comprises bismaleimide.

8. The semiconductor device of claim 7, wherein said adhesive layer consists essentially of bismaleimide.

9. The semiconductor device of claim 1, wherein said adhesive comprises initiators which react at a temperature below about 100°C.

10. The semiconductor device of claim 1, further comprising electrical contacts on said solder mask and said die, each said contact on said die being wire bonded to a respective said contact on said solder mask.

11. The semiconductor device of claim 10, wherein said contacts are substantially free of contaminants from said adhesive layer.

12. A semiconductor device comprising:

a solder mask;

a die;

electrical contacts on said solder mask and said die, each said contact on said die being wire bonded to a respective said contact on said mask, and

an adhesive layer affixing said die to said solder mask, wherein said adhesive layer is cured at a temperature between about 20°C and about 50° C higher than a glassy temperature of said adhesive layer and said curing temperature is below about 100°C.

13. The semiconductor device of claim 12, wherein said adhesive layer is at least partially cured at a temperature below about 100°.

14. The semiconductor device of claim 13, wherein said adhesive layer is at least fifty percent cured at a temperature below about 100°C.

15. The semiconductor device of claim 12, wherein said adhesive layer is cured at a temperature below about 85°C.

16. The semiconductor device of claim 15, wherein said adhesive layer comprises a material with a glassy temperature between about 5°C and about 20°C.

17. The semiconductor device of claim 16, wherein said adhesive layer comprises bismaleimide.

18. The semiconductor device of claim 17, wherein said adhesive layer consists essentially of bismaleimide.

19. The semiconductor device of claim 12, wherein said adhesive comprises initiators which react at a temperature below about 100°C.

20. The semiconductor device of claim 12, wherein said contacts remain relatively free of contaminants released during a cure process.

21. A method of making a semiconductor device comprising:

affixing a solder mask to a semiconductor die with an adhesive layer; and

at least partially curing said adhesive layer by exposing said adhesive layer to a temperature no greater than 100°C.

22. The method of claim 21, further comprising:

electrically connecting contacts on said die with contacts on said solder

mask;

attaching a chip to said solder mask; and

encapsulating said die; solder mask and chip with a mold.

23. The method of claim 23, wherein said mold encapsulates at a temperature of greater than about 100°C.

24. The method of claim 23, wherein said mold encapsulates at a temperature of about 180°C.

25. The method of claim 23, further comprising curing said mold.

26. The method of claim 25, wherein said mold curing is at about 175°C.

27. The method of claim 21, wherein said adhesive layer is partially cured at a temperature below about 100°.

28. The method of claim 27, wherein said adhesive layer is at least fifty percent cured at a temperature below about 100°C.

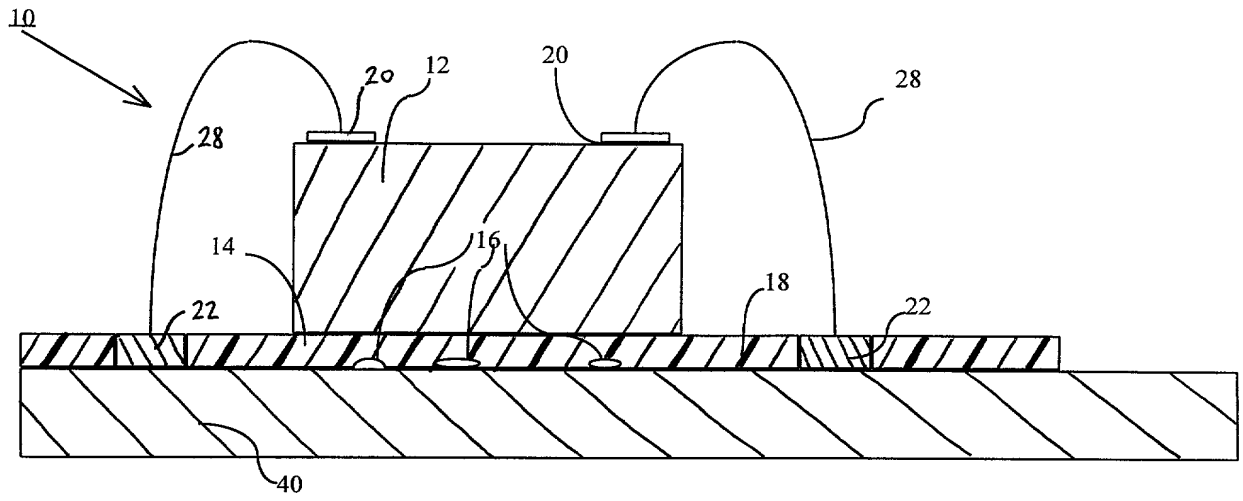
29. The method of claim 21, wherein said adhesive layer is cured at a temperature between about 20°C and about 50° C higher than glassy temperature of said adhesive layer.

30. The method of claim 29, wherein said adhesive layer is cured at a temperature below about 85°C.

ABSTRACT

A low temperature cure adhesive material for affixing a solder mask to a die is described. The adhesive material is at least partially cured at temperatures below about 100°C. The low temperature curing lowers the thermal stresses on the adhesive, diminishes the possibility of voids being formed in the adhesive material, and increases the bond yield.

FIG. 1



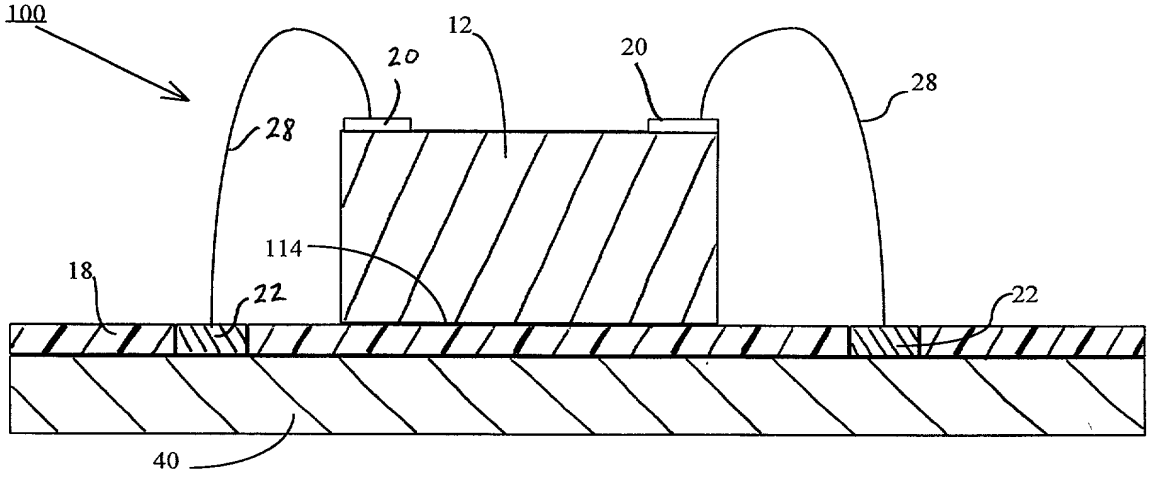
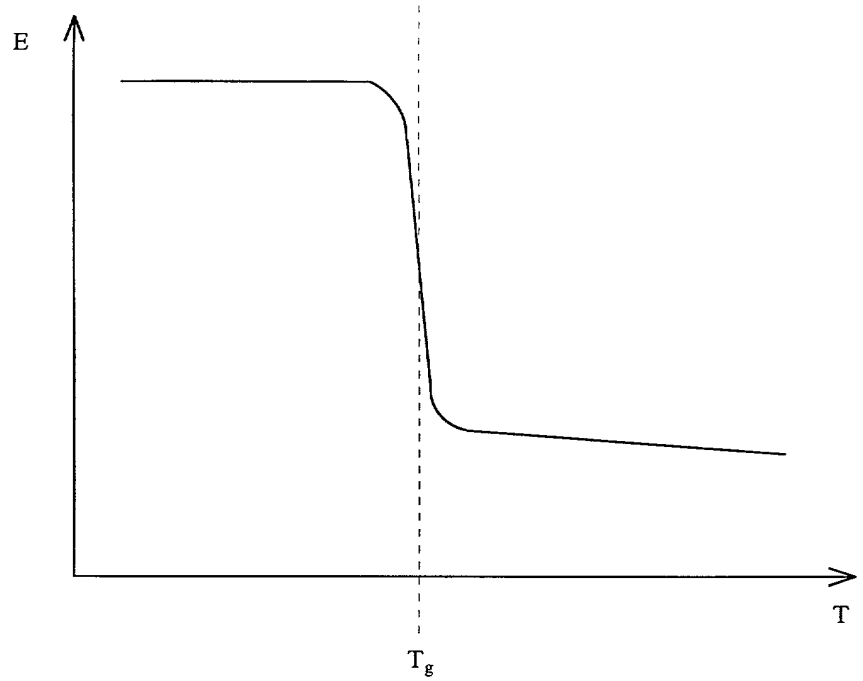


FIG. 2

FIG. 3



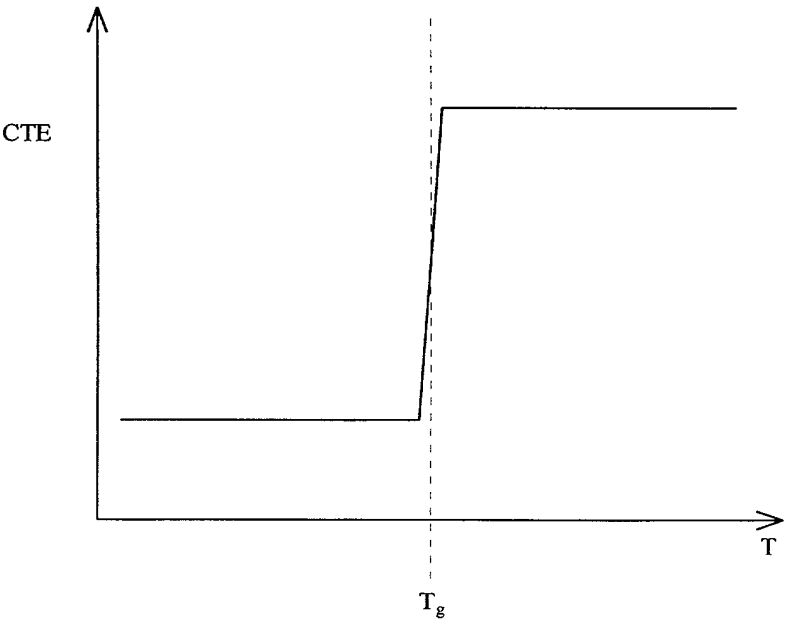


FIG. 4

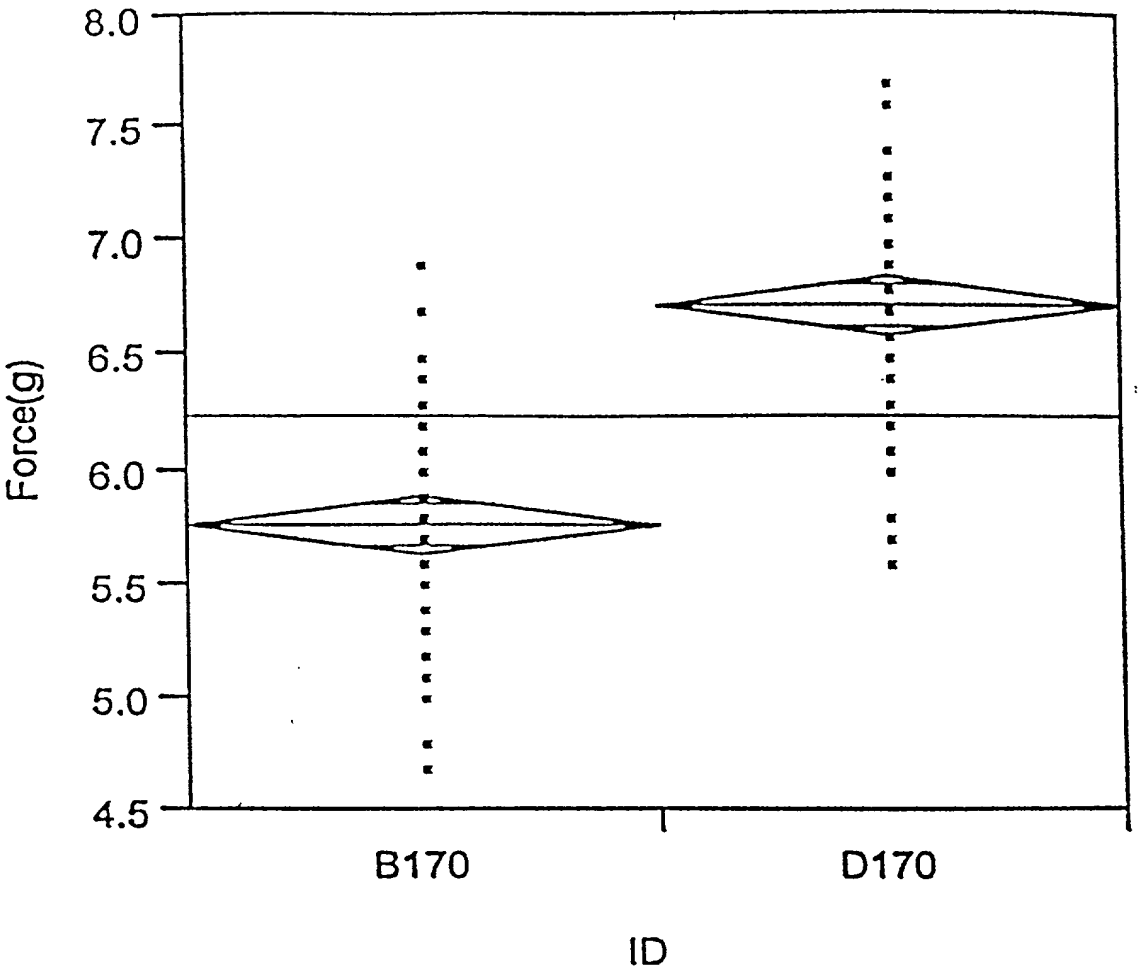


FIG. 5

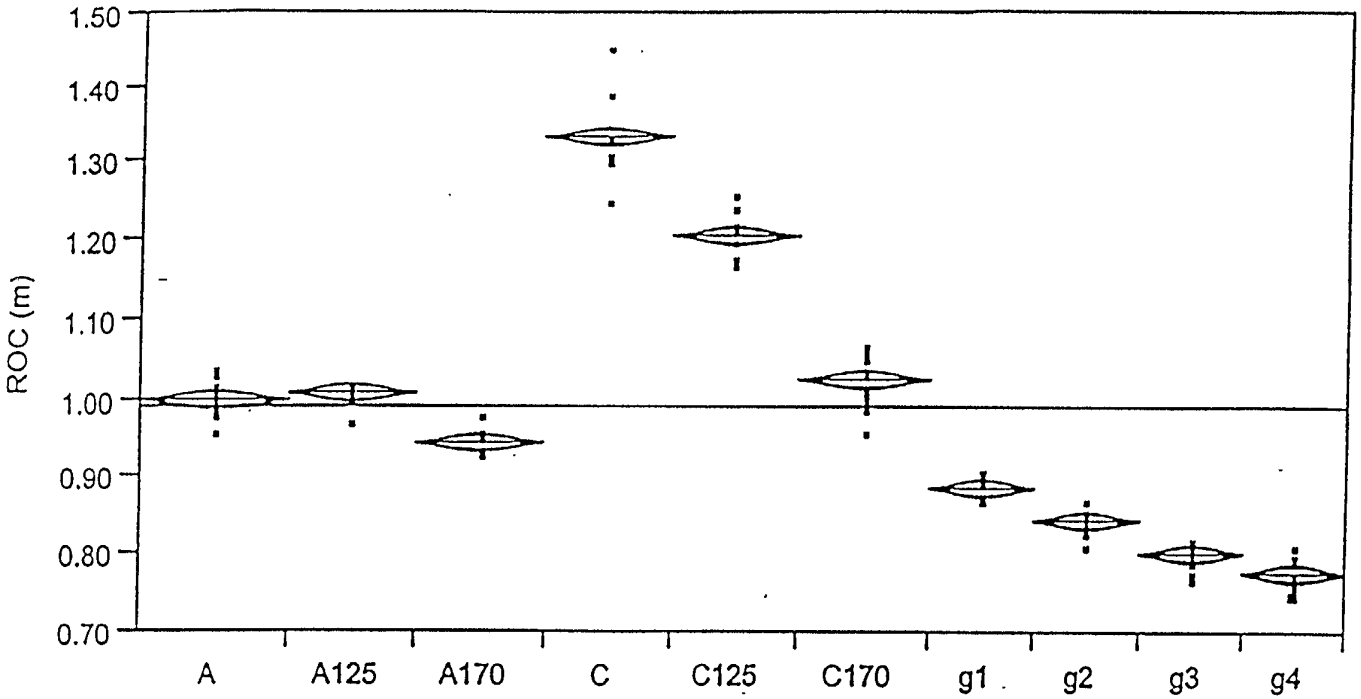
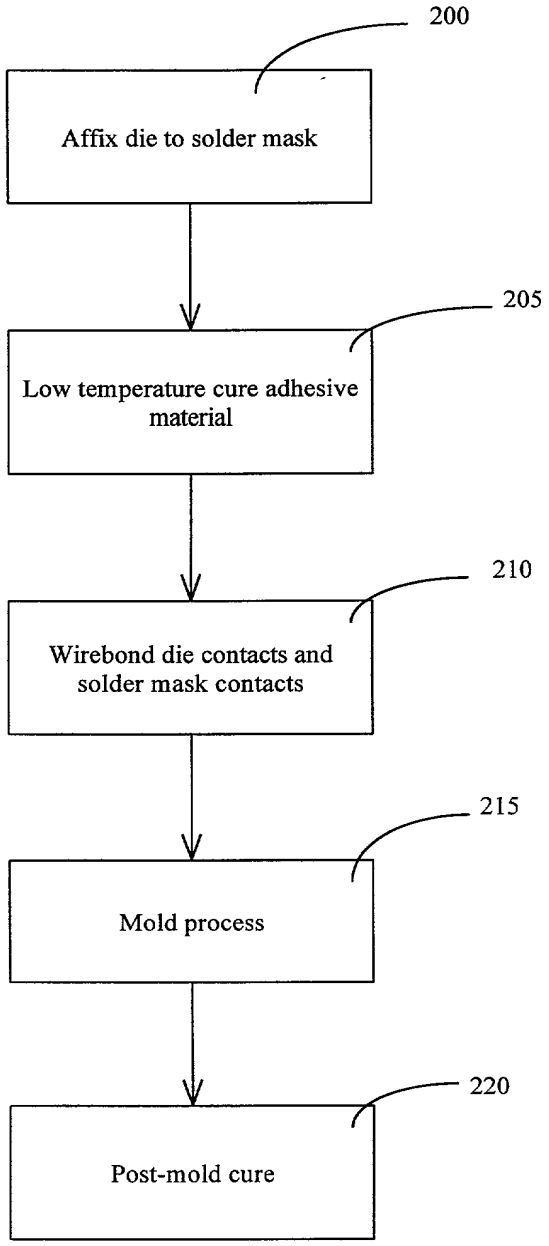

1.50
1.40
1.30
1.20
1.10
1.00
0.90
0.80
0.70
ROC (m)
A
A125
A170
C
C125
C170
g1
g2
g3
g4

FIG. 6

FIG. 7


200
Affix die to solder mask
205
Low temperature cure adhesive material
210
Wirebond die contacts and solder mask contacts
215
Mold process
220
Post-mold cure

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DECLARATION FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled:

DIE ATTACH CURING METHOD FOR SEMICONDUCTOR DEVICE

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by an amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose all information known to me which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐
_____ (Number)	_____ (Country)	_____ (Filing Date)	☐

I hereby claim the benefit under Title 35, United States Code, § 120/365 of any United States and PCT international application(s) listed below and, insofar as the

subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Please address all correspondence to Thomas J. D'Amico of Dickstein Shapiro Morin & Oshinsky LLP located at 2101 L Street NW, Washington, DC 20037-1526. Telephone calls should be made to (202) 785-9700.

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Inventor's signature: _____ Date: 1/11/00
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Citizenship: ~~China~~ US TB
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Docket No.: M4065.0226/P226
Micron No.: 98-956

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Tongbi Jiang

Serial No.: Not Yet Assigned

Group Art Unit: Not Yet Assigned

Filed: Concurrently Herewith

Examiner: Not Yet Assigned

For: DIE ATTACH CURING METHOD FOR SEMICONDUCTOR DEVICE

Assistant Commissioner for Patents
Washington, D.C. 20231

POWER OF ATTORNEY BY ASSIGNEE AND CERTIFICATE BY ASSIGNEE UNDER 37 CFR § 3.73(b)

Micron Technology, Inc., Assignee of the entire right, title and interest in the above-identified application by virtue of the Assignment attached hereto (which is also being submitted concurrently for recordation), hereby appoints the attorneys and agents of the firm of located at , listed as follows: Gary M. Hoffman, 26,411; Thomas J. D'Amico, 28,371; Donald A. Gregory, 28,954; James W. Brady Jr., 32,115; Jon D. Grossman, 32,699; Mark J. Thronson, 33,082; Jeremy A. Cubert, 40,399; Laurence E. Fisher, 37,131; Brian A. Lemm, 43,748; Gianni Minutoli, 41,198; Edwin Oh, P-45,319; Eric Oliver, 35,307; William E. Powell III, 39,803; Paul L. Ratcliffe, P-45,290; Mark E. Strickland, 45,138 and Salvatore P. Tamburo, P-45,153, and also attorneys of Micron Technology, Inc. as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

The Assignee certifies that the above-identified assignment has been reviewed and to the best of the Assignee's knowledge and belief, title is in the assignee.

Please direct all correspondence regarding this application to the following:

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MICRON TECHNOLOGY, INC.

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Registration No. 30,871

Dated: 1-12-00